What is claimed is:

1. An apparatus connectable to a computer network for circuit design verification comprising:

a verification result collector configured to collect a verification result of a circuit;

a data conversion and registration module configured to convert the verification result to a pre-analysis indication file;

an analysis information collector configured to collect analysis information about a redundant non-active portion of the circuit;

an analysis information processor configured to exclude an affect of the redundant non-active portion from the verification result and make a analysis indication file;

an indication file storage portion configured to store the pre-analysis indication file and the analysis indication file; and

a data indication controller configured to output the pre-analysis indication file and the analysis indication file.

2. The apparatus of claim 1, further comprising a file combining module configured to combine the pre-analysis indication file and the analysis indication file.

3. The apparatus of claim 1, further comprising:

a criterion data collector configured to collect a quality standard of the circuit; and

a criterion data storage portion configured to store the quality standard.

4. The apparatus of claim 1, wherein the data indication controller further comprises a data discriminator configured to extract an item failing the quality standard from the analysis indication file.

5. The apparatus of claim 1, further comprising a data processor configured to extract information of a common non-active portion from the pre-analysis indication file and the verification result.

6. The apparatus of claim 1, wherein the verification result is at least one of an RTL code coverage and a fault detecting ratio.

7. A computer implemented method for design verification comprising:

collecting a verification result of a circuit through a computer network;

converting the verification result to a pre-analysis indication file and storing the pre-analysis indication file in an indication file storage portion;

collecting analysis information about a redundant non-active portion of the circuit through the computer network;

excluding an affect of the redundant non-active portion from the verification result and making an analysis indication file; and

storing the analysis indication file in the indication file storage portion.

8. The method of claim 7, further comprising instructing a display device to show the pre-analysis indication file and the analysis indication file.

9. The method of claim 7, further comprising combining the pre-analysis indication file and the analysis indication file.

10. The method of claim 7, further comprising extracting information of a common non-active portion from the pre-analysis indication file and the verification result.

11. The method of claim 7, wherein the verification result is at least one of an RTL code coverage and a fault detecting ratio.

12. A computer program product for controlling a computer

system so as to verify circuit designs, the computer program product comprising:

instructions configured to collect a verification result of a circuit through a computer network;

instructions configured to collect analysis information about a redundant non-active portion of the circuit through the computer network;

instructions configured to exclude an affect of the redundant non-active portion from the verification result and making an analysis indication file within the computer system; and

instructions configured to store the analysis indication file in the indication file storage portion within the computer system.

13. The computer program product of claim 12, further comprising instructions configured to show the pre-analysis indication file and the analysis indication file by a display device.

14. The computer program product of claim 12, further comprising instructions configured to combine the pre-analysis indication file and the analysis indication file within the computer system.

15. The computer program product of claim 12, further

comprising instructions configured to extract information of a common non-active portion from the pre-analysis indication file and the verification result.

16. The computer program product of claim 12, wherein the verification result is at least one of an RTL code coverage and a fault detecting ratio.

17. A computer implemented method for manufacturing an integrated circuit comprising:

sending a verification result of a circuit design to an apparatus for circuit design verification through a computer network;

instructing the apparatus to convert the verification result to a pre-analysis indication file and store the pre-analysis indication file in an indication file storage portion;

sending analysis information about a redundant non-active portion of the circuit design to the apparatus through the computer network;

instructing the apparatus to exclude an affect of the redundant non-active portion from the verification result and make an analysis indication file;

instructing the apparatus to store the analysis indication file in the indication file storage portion;

receiving the analysis indication file from the